REMARKS

The present response amends claims 1 and 16 in conformity with the following remarks. In addition, claim 2 has been canceled without prejudice or disclaimer as to the subject matter recited therein. Claims 1 and 3-20 remain pending in the captioned case. Further examination and reconsideration are respectfully requested.

Objection to the Drawings

Applicants acknowledge the informality of the present drawings, and agree that formalized replacement drawings will be filed once the application is allowed.

Sections 102/103 Rejections

Claims 1-2 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,231,598 to Vlahos (hereinafter "Vlahos"). Claims 3-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Vlahos in view of U.S. Patent No. 6,671,860 to Langford, II (hereinafter "Langford").

The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art of reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); MPEP 2131. Furthermore, anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, as arranged in the claim. *W.L. Gore & Assocs. V. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983). Using these standards, Applicants submit the cited art fails to disclose each and every element of the currently pending claims, some distinctive features of which are set forth in more detail below.

To establish a case of *prima facie* obviousness of a claimed invention, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Second,

there must be a reasonable expectation of success. As stated in MPEP 2143.01, the fact that references can be hypothetically combined or modified is not sufficient to establish a *prima facie* case of obviousness. *See In re Mills*, 916 F.2d. 680 (Fed. Cir. 1990). Finally, the prior art references must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d. 981 (CCPA 1974); MPEP 2143.03. Specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d., 1382 (CCPA 1970). Using these standards, Applicants contend that the cited art fails to teach or suggest all features of the currently pending claims, some distinctive features of which are set forth in more detail below.

Neither Vlahos nor Langford, either singularly or in combination, teach an output signal sent directly from a circuit (DUT) to a logic gate absent any circuitry beyond the logic gate coupled for receiving that output signal. Amended claim 1 recites a logic gate placed within a functional path extending from a DUT to a bonding pad of an integrated circuit. The logic gate can be reference 40, and the functional path can be reference 18 extending from a DUT output to bonding pad 20 (Specification -- Fig. 3).

In order to properly characterize the operation of a DUT, it is important that the loading on the output of the DUT be minimized (Specification -- pg. 7, lines 25-31). Minimal loading is especially important when measuring the skew or access times of a DUT. If the output signal extending from a DUT "sees" two loads or significant circuitry with impedance connected to the DUT output, the skew test results will be unduly high (Specification -- pg. 8, lines 1-7).

To minimize skew test results and gain a more accurate access time measurement, "the output signal of Fig. 3 is sent only into an input of EX OR gate 40" (Specification -- pg. 9, lines 5-6, emphasis added; Fig. 3). Placing the output signal from the DUT directly onto only one input of a logic gate absent any circuitry beyond that logic gate coupled to receive the output signal minimizes additional skewing and access time delays when it is desirable to measure DUT performance (Specification -- pg. 10, lines 27-30). A comparison of Figs. 2-3 of the present specification makes clear that if only the logic gate 40 is placed on the output signal A_DUT_{OUT} of functional path 18, skewing is minimized and measurement is more accurate.

Contrary to present claim 1, the output from DUT 25 of Vlahos goes through multiple circuitry before reaching comparator 45 (Vlahos -- Fig. 2). Specifically, filter 28, switch 30, splitting network 32, amplifiers 34/35, tunnel diode circuits 40, and switch 44 all add loading to the output signal to increase the skew amounts (Vlahos -- Fig. 2). Since Vlahos works in a feedback arrangement with the output sent to microcontroller 12 rather than to a bonding pad of an integrated circuit, additional skewing can be compensated for in the feedback loop. Therefore, one skilled in the art would readily discern that additional loading need not be minimized in Vlahos since the feedback will compensate for such additional skewing. A skilled artisan would also recognize that the presently claimed signal skew measuring device does require minimal skewing by minimizing the load that the output signal sees, and the only circuitry which the output signal is sent is the claimed logic gate.

The shortcomings of Vlahos are compounded in Langford. Nowhere in Langford is there any mention of an output signal from a DUT. Instead, Langford describes a boundary scan cell architecture for use in testing integrated circuits according to the IEEE Standard 1149.1 Test Access Port (TAP), oftentimes referred to as JTAG testing. Absent description of a DUT, Langford makes no mention of an output signal from that DUT or an output signal sent only to a logic gate.

Neither Vlahos nor Langford, either singularly or combination, teach a functional path extending between the DUT and the bonding pad of an integrated circuit. Present claim 1 notes that the claimed logic gate is placed within a functional path and that the functional path extends from the DUT to a bonding pad of an integrated circuit. A bonding pad is well-known to those skilled in the art as one in which the integrated circuit is coupled to a device external to the integrated circuit on, for example, a multi-chip package or printed circuit board. Support for the amendment to claim 1 is set forth in the original specification, for example, page 4, lines 29-33.

Contrary to present claim 1, Vlahos makes no mention of a bonding pad. Instead, the output from logic gate 45 of Vlahos is sent to a microcontroller 12, known to a skilled artisan as an electronic subsystem placed on the same integrated circuit as that which contains the other components shown in Fig. 2 of Vlahos. Absent any description that the output signal from logic gate

45 is sent to a bonding pad, Applicants assert that Vlahos cannot teach the limitations of present claim 1.

The shortcomings of Vlahos are also deficient in Langford. If XOR gate 400 of Langford is the claimed logic gate, it is clear that the output from gate 400 is fed to a multiplexer 106, not the claimed latch (Langford -- Fig. 4). Moreover, it is clear that the output from multiplexer 106 of Langford does not couple to a bonding pad. Instead, the output from multiplexer 106 of Langford is sent as a SIGNAL_OUT, which is not terminated with a bonding pad (Langford -- Fig. 4).

Neither Vlahos or Langford, either singularly or in combination, teach a first series-connected logic gate and latch for latching a transition of a clock signal and a second series-connected logic gate and latch for latching a transition of an output signal. Claim 8 describes two series-connected elements. The first series-connected logic gate and latch is coupled to receive a clock signal, such as DUT_{CLK}, and to latch a transition of that clock signal. An illustration of the first series-connected logic gate and latch is set forth in present Fig. 4. The second series-connected logic gate and latch receives an output signal, such as A_DUT_{OUT}, from the circuit or DUT. The second series-connected logic gate and latch can also receive an expected output signal or E_DUT_{OUT}, and to latch a transition of the output signal A_DUT_{OUT}. An illustration of the second series-connected logic gate and latch is set forth in present Fig. 3. The combination of Figs. 3 and 4 define a transition of clock signal DUT_{CLK} and transition of an output signal A_DUT_{OUT}. That combination can be used to derive the delay or skew of the DUT by looking at how much longer it would take for the output signal to appear after the clock signal occurs (Specification -- Fig. 5).

Contrary to claim 8, while Vlahos may teach a single series-connected logic gate 45 and latch 50 for latching a transition of an output signal to be fed to microcontroller 12 (Vlahos -- Fig. 2), nowhere in Vlahos is there any mention of a second series-connected logic gate and latch. If the Examiner is assuming that Langford describes a first series-connected logic gate and latch, it is imperative to note that the claimed first series-connected logic gate and latch must latch a transition of a clock signal. However, logic gate 400 and latch 102 do not receive clock signals (Langford -- Fig. 4). Instead, latch 102 receives SIGNAL_IN as does logic gate 400 (Langford -- Fig. 4). A skilled artisan would certainly know the difference between a signal and a clock, such as CLK_DR

158 (Langford -- Fig. 4). Like Vlahos, Langford makes no mention of a first series-connected logic gate and latch coupled for latching a transition of a clock signal.

Neither Vlahos nor Langford, either singularly or in combination, teach a delay measurement device coupled for measuring the difference between transitions of the clock signal and the output signal. Independent claims 8 and 16 each describe measuring a time difference between transition of a clock signal and transition of an output signal.

While Vlahos teaches a skew tester 60, skew tester 60 only measures phase difference between a digital sine wave at, for example, 1.9043487 Mhz and a clock signal frequency of 30.517579 Mhz using what is known as a selectable phase number (Vlahos -- col. 7, lines 31-59). The selectable phase number is chosen in the feedback path by microcontroller 12 and stored in a Phase Increment Register A (PIRA) on both channels 1 and 2 (Vlahos -- Fig. 4; col. 8, lines 53-69). Microcontroller 12 can then set the skew number based on a threshold value of detector circuit 50 for stepping the phase of the measurement signal, all of which result in skew testing and measurement using only a single series-connected logic gate and latch, and absent any delaying measurement device coupled to receiving transitions of a clock signal and the output signal as presently claimed.

For at least the reasons stated above, Applicants believe independent claims 1, 8, and 16, as well as claims dependent therefrom, are patentably distinct over Vlahos and Langford. In addition, claim 2 has been canceled rendering rejection thereto moot. Accordingly, Applicants respectfully request removal of this rejection.

CONCLUSION

The present amendment and response is believed to be a complete response to the issues raised in the Office Action mailed July 26, 2006. In view of the remarks herein, Applicants assert that pending claims 1 and 3-20 are in condition for allowance. If the Examiner has any questions, comments or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to LSI Logic Corporation Deposit Account No. 12-2252.

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